Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov/Dec– 2017**

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| **Code :** | **17EC3031** | **Duration :** | **3hrs** |
| **Sub. Name :** | **DIGITAL SYSTEM AND ASIC DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Design a sequence detector using JK FF that produces an output 1 whenever the sequence 1011 is detected. | CO1 | 15 |
| b. | Explain a priority encoder with neat diagram. | CO1 | 5 |
| (OR) | | | | |
| 2. | a. | Design a decade counter using JK FFs and T FFs. | CO1 | 15 |
| b. | Sketch the circuit of a 2-bit magnitude comparator. | CO1 | 5 |
|  |  |  |  |  |
| 3. |  | Design a Vending Machine Controller using DFFs and PLA. | CO2 | 20 |
| (OR) | | | | |
| 4. | a. | Apply the following Boolean functions in PAL.  W(A,B,C,D) = ∑ (1,3,4,6,12) X(A,B,C,D) = ∑ (7,8,9,10,11,12,13) Y(A,B,C,D) = ∑ (0,2,3,4,5,6,7,8,12) Z(A,B,C,D) = ∑ (1,2,8,12,13,14,15) | CO2 | 10 |
|  | b. | Design a BCD to Gray code converter using PAL. | CO2 | 10 |
|  |  |  |  |  |
| 5. |  | Define the design rules for a CMOS process using neat diagrams. | CO3 | 20 |
| (OR) | | | | |
| 6. | a. | Apply the following functions using CMOS logic cells. | CO3 | 10 |
|  | b. | Describe a delay model of a 3-input NOR logic cell based on logical effort. | CO3 | 10 |
|  |  |  |  |  |
| 7. | a. | Explain the programming technology used in Altera MAX 5000 EPLDs and Xilinx EPLDs. | CO4 | 8 |
|  | b. | Analyze the Actel ACT 1 architecture and its timing model with neat diagrams. | CO4 | 12 |
| (OR) | | | | |
| 8. | a. | Analyze the Xilinx LCA interconnect with neat diagrams. | CO5 | 12 |
|  | b. | Demonstrate the interconnect schemes in Altera MAX 7000 and MAX 9000. | CO5 | 8 |
|  | |  |  |  |
|  | | **Compulsory**: |  |  |
| 9. | a. | Illustrate the Schematic-entry tools for ASIC design with neat diagrams. | CO5 | 14 |
|  | b. | Demonstrate the CFI Design with an example. | CO6 | 6 |

ALL THE BEST